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US 4674173 A

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UK CL (Edition N) H1K KAAL KAAP KAAX
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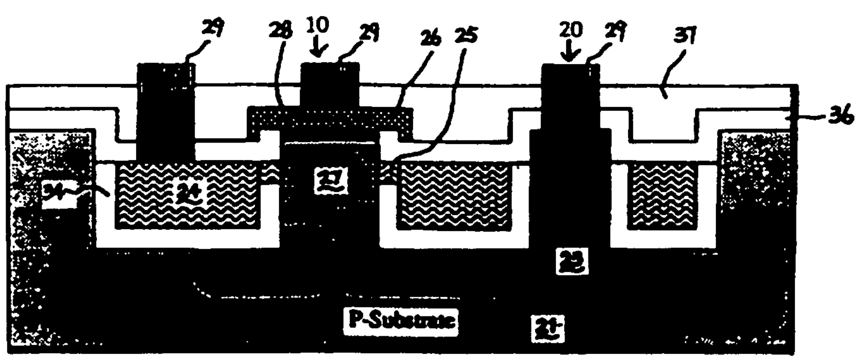
Online : WPI

(54) **Pillar bipolar transistors**

(57) A pillar bipolar transistor which has a bidirectional operation characteristic in which the parasitic junction capacitance of a base electrode is reduced. A method for fabricating the transistor comprises etching a substrate (21) using a first patterned insulating layer (32) as a mask to form first and second pillars (10, 20) separated by a trench injecting an impurity using a mask (33, 32) to form a collector (23) under the first and second pillars and in the second pillar (20); depositing a first oxide layer (34) and a first polysilicon layer (24') polishing the first polysilicon layer using the first oxide layer as a polishing stopper; removing a portion of the first polysilicon layer and a portion of the first oxide layer to define an extrinsic base (24); etching the oxide layer formed on both sides of the first pillar to a predetermined depth to define a connecting portion and forming buried polysilicon to form the connection portion (25); depositing a second oxide layer (36) and a second polysilicon layer (35) polishing the second polysilicon layer using the second oxide layer as a polishing stopper; removing only the second oxide layer formed on the top of the first pillar to expose a surface of the first pillar; injecting an impurity in the first pillar to form a base (27) at a centre portion; injecting an impurity to form an emitter (28) at an upper portion of the first pillar; depositing a third polysilicon layer (26) on the emitter, the third polysilicon layer being formed on an area wider than the emitter; and forming self-aligned contact holes to form electrodes (29) through the contact holes.

FIG.3



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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

FIG.1
(PRIOR ART)

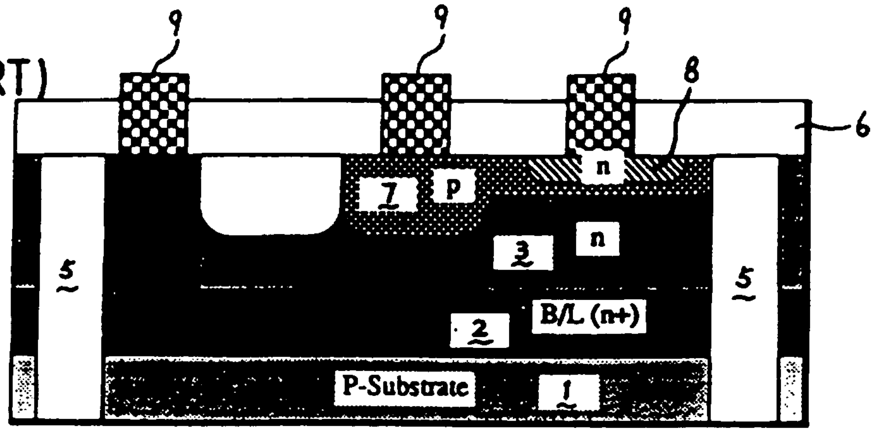


FIG.2
(PRIOR ART)

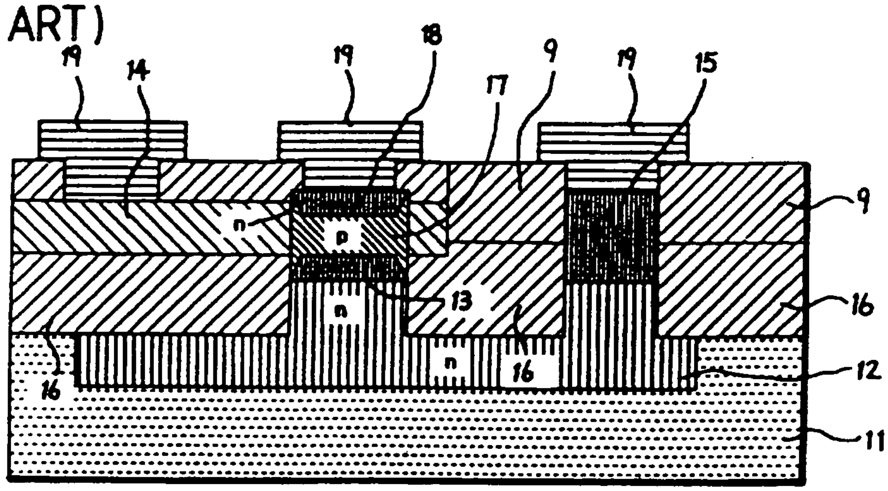


FIG.3

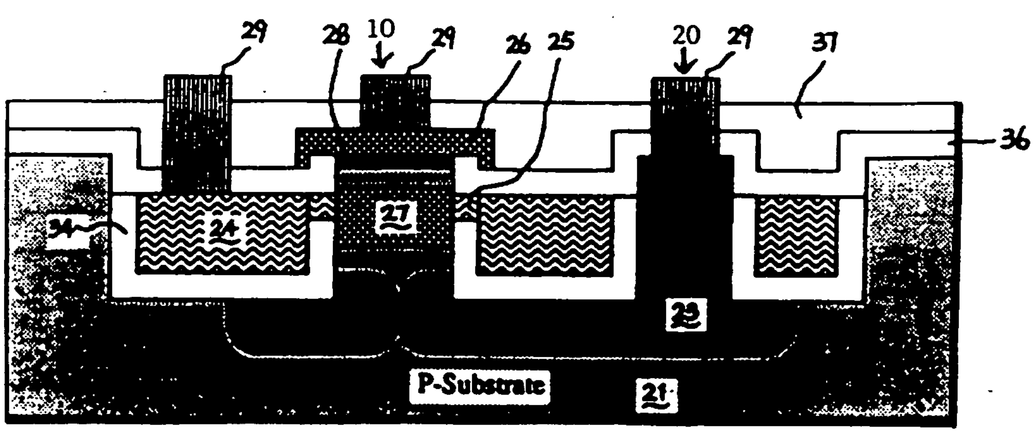


FIG.4A

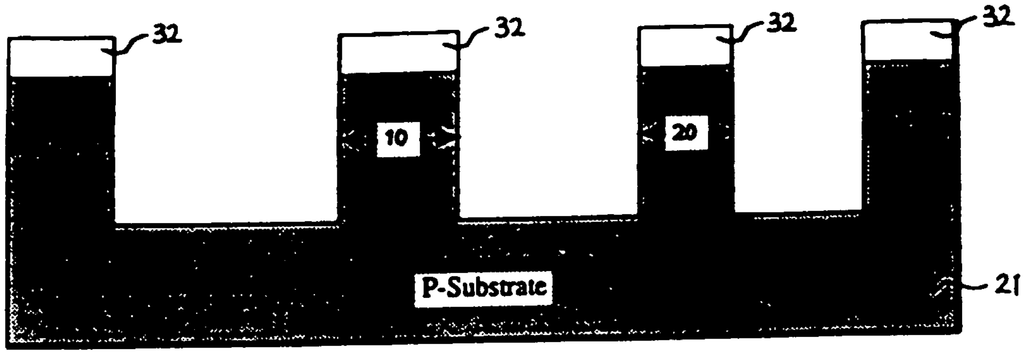


FIG.4B

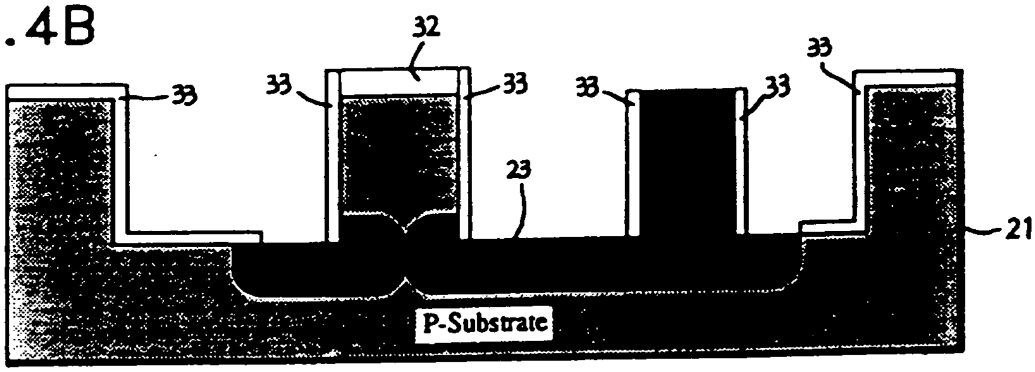


FIG.4C

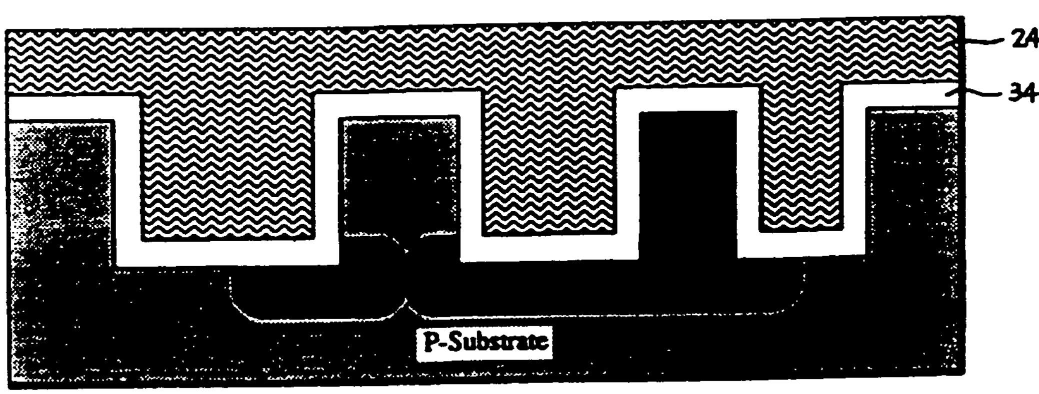


FIG.4D

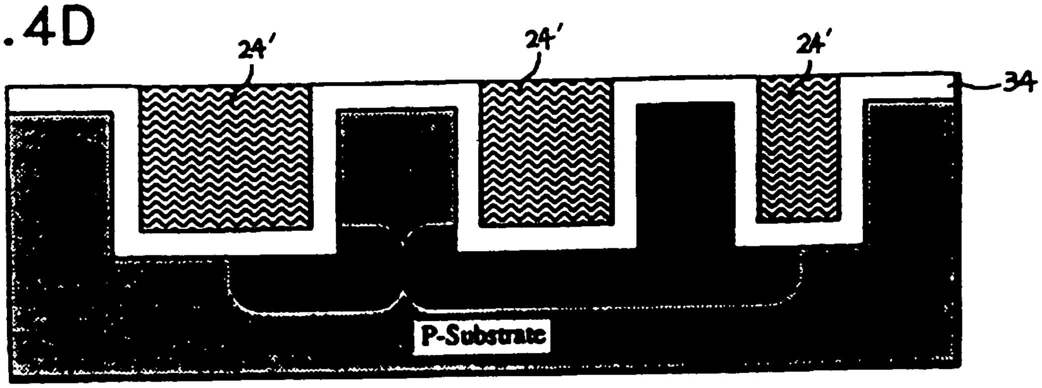


FIG.4E

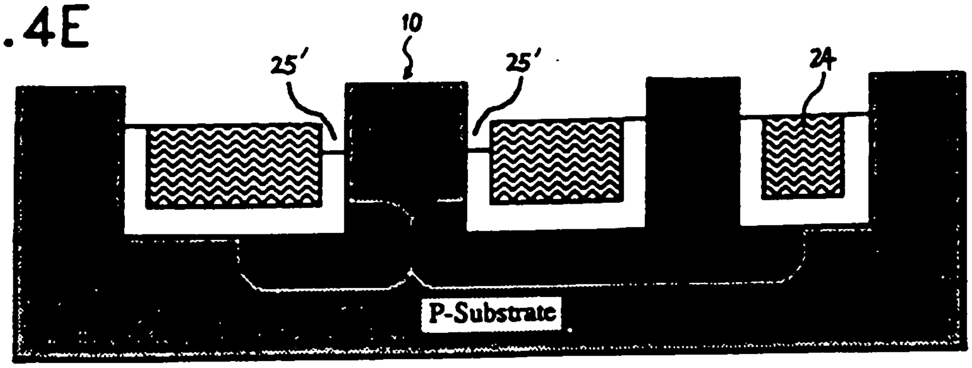


FIG.4F

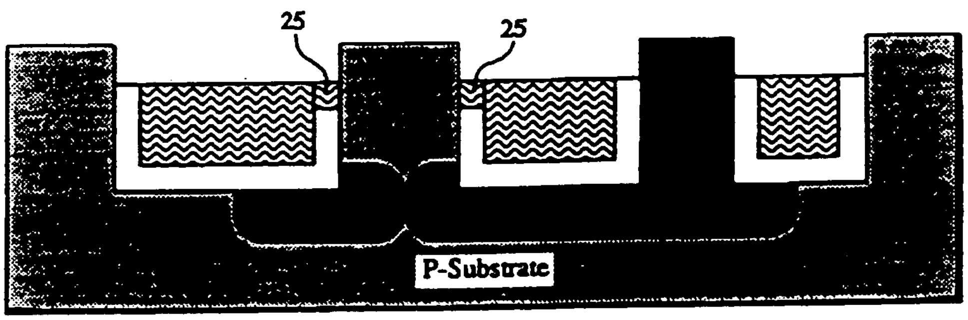


FIG.4G

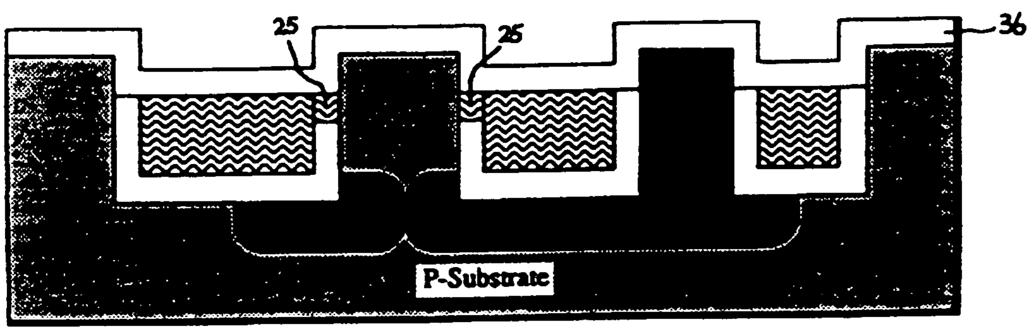


FIG.4H

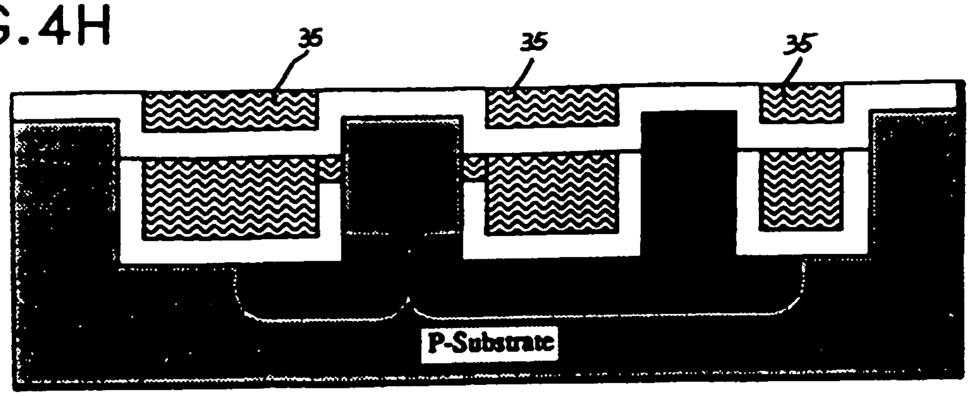


FIG.4I

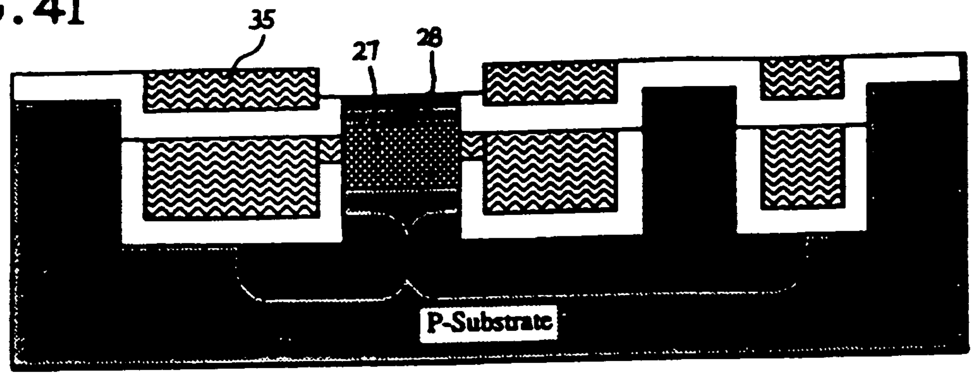


FIG.4J

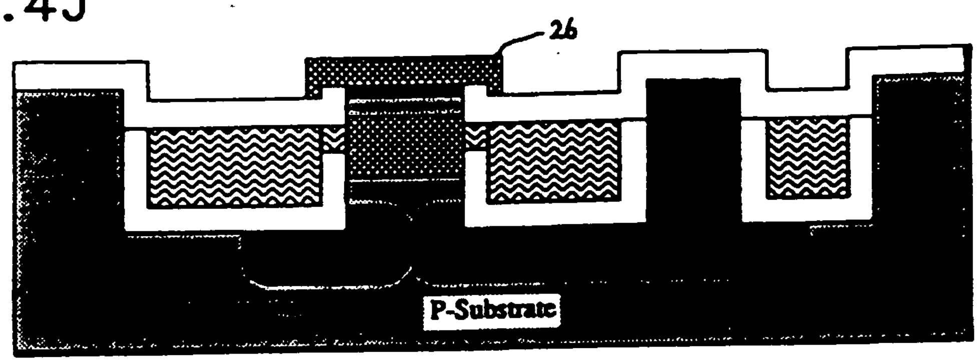
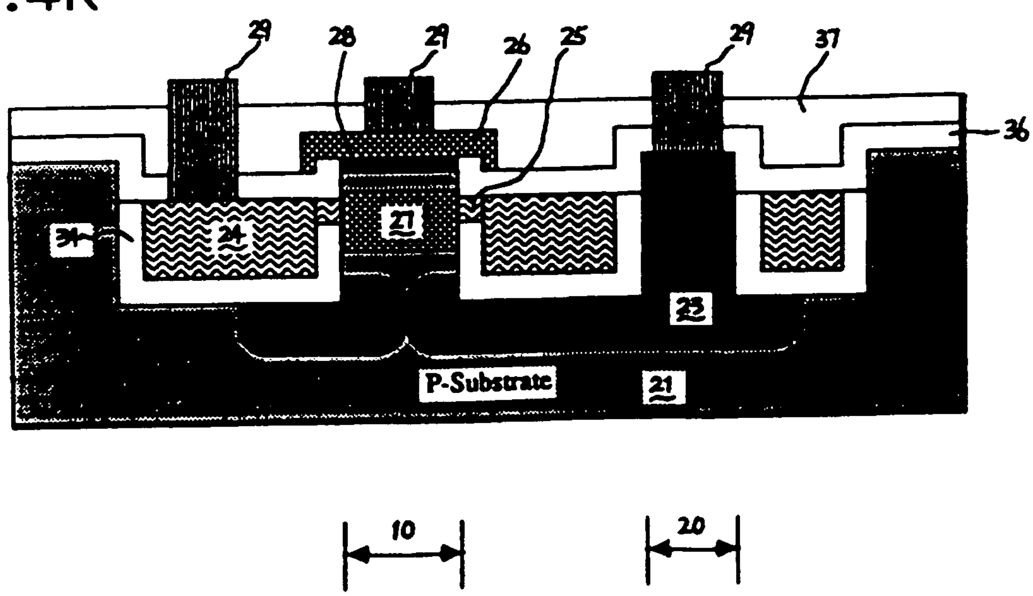


FIG.4K



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PILLAR BIPOLAR TRANSISTORS

The present invention relates to semiconductor devices, and more particularly to pillar bipolar transistors which have a bidirectional operation characteristic.

As integration of a semiconductor device is improved, the driving speed and current gain thereof are enhanced, but the operation characteristics thereof are still somewhat restricted.

Figure 1 of the accompanying drawings is a cross-sectional view showing the construction of a bipolar transistor which is fabricated by a previously proposed technique.

This technique seeks to provide that the parasitic junction capacitance of a collector 3, i.e. the parasitic junction capacitance between the substrate 1 and the buried collector 2, is reduced and the size of the bipolar transistor is further reduced.

In Figure 1, reference numeral 6 indicates an insulating layer, reference numeral 7 indicates a base region, and reference numerals 8 and 9 indicate an emitter region and an electrode, respectively.

In the bipolar transistor of Figure 1, since the base region 7 is wide and the emitter and base regions 8, 7 are joined with each other at areas of high concentration, there arises the problem that the power consumption is large.

Also, in order to enhance the operation characteristics, the construction of pillar bipolar transistors is known. An example of such is disclosed in Europe Published Patent Application EP-A-0140369 and is as shown in Figure 2 of the accompanying drawings.

With reference to Figure 2, the method for fabricating the disclosed pillar bipolar transistor comprises the steps of selectively etching a single crystal semiconductor substrate 11 to form pillars therein, forming an emitter region 18, a base region 17, a collector region 13 and collector sinker region 15 in the pillars, isolating active regions by a buried insulating layer 16, and forming a polysilicon layer 14 as an extrinsic base region at both sides of one of the pillars to complete fabrication of a pillar bipolar transistor.

In the pillar bipolar transistor fabricated by the above method, however, since the polysilicon layer 14 is connected with both sides of the pillar in which the base region 17 is formed, the base region 17

becomes large. Thus, the operation characteristic of the pillar bipolar transistor is lowered.

Additionally, since the emitter and collector regions must be formed at an upper portion of the pillar, there arises the problem that it is extremely difficult to perform a self-aligned contact open process.

The present invention seeks to provide a pillar bipolar transistor which has a bidirectional operation characteristic and in which the parasitic junction capacitance between the base and the collector or between the base and the emitter can be reduced.

The present invention also seeks to provide a method of fabricating a pillar bipolar transistor in which it is easier to form an extrinsic base region in electrical connection with a base region formed in a pillar and form a self-aligned contact opening for interconnection.

According to one aspect of the present invention there is provided a pillar bipolar transistor, comprising:

a semiconductor substrate of a first conductivity type having at least three trench regions, and first and second pillar structures formed between the trench regions;

a collector region formed under the first and second pillar structures and in the second pillar structure, and doped with an impurity of a second conductivity type;

a extrinsic base region buried in the trench regions;

an oxide layer formed between the extrinsic base region and the substrate;

an intrinsic base region of the first conductivity type formed at a centre portion of the first pillar structure;

a connecting portion formed between the extrinsic base region the intrinsic base region to electrically connect the extrinsic base region with the intrinsic base region;

an emitter region of the second conductivity type formed at an upper portion of the first pillar structure; and

electrodes formed through contact holes on the emitter, collector and base region.

Preferably, the transistor further comprises a conductive thin film wider than and formed on top of the emitter so as to make

formation of a contact hole easier.

In preferred embodiments, the conductive thin film is composed of polysilicon containing an impurity of the second conductivity type.

Preferably, the extrinsic base region is composed of polysilicon.

According to another aspect of the present invention there is provided a pillar bipolar transistor, comprising:

a semiconductor substrate of a first conductivity type having at least three trench regions, and first and second pillar structures formed between the trench regions;

an emitter region formed under the first and second pillar structures and in the second pillar structure, and doped with an impurity of a second conductivity type.

an extrinsic base region buried in the trench regions;

an oxide layer formed between the extrinsic base region and the substrate;

an intrinsic base region of the first conductivity type formed at a centre portion of the first pillar structure;

a connection portion formed between the extrinsic base region the intrinsic base region to electrically connect the extrinsic base region with the intrinsic base region;

a collector region of the second conductivity type formed at an upper portion of the first pillar structure; and

electrodes formed through contact holes on the emitter, collector and base region.

According to a further another aspect of the present invention there is provided a method of fabricating a pillar bipolar transistor, the method comprising the steps of:

etching a silicon substrate of a first conductivity type using a first patterned insulating layer as a mask to form first and second pillar structures separated by a trench region therein;

injecting an impurity of a second conductivity type using a second patterned insulating layer as a mask to form a collector region under the first and second pillar structures and in the second pillar structure;

sequentially depositing a first oxide layer and a first polysilicon layer thereon;

polishing the first polysilicon layer using the first oxide layer

as a polishing stopper;

removing a portion of the first polysilicon layer and a portion of the first oxide layer to define an extrinsic base region;

etching the oxide layer formed on both sides of the first pillar structure to a predetermined depth to define a connecting portion and forming a buried polysilicon therein to form the connection portion;

sequentially depositing a second oxide layer and a second polysilicon layer thereon;

polishing the second polysilicon layer using the second oxide layer as a polishing stopper;

removing only the second oxide layer formed on top of the first pillar structure to expose a surface of the first pillar structure;

injecting an impurity of the first conductivity type in the first pillar structure to form a base region at a centre portion thereof;

injecting an impurity of the second conductivity type to form an emitter region at an upper portion of the first pillar structure;

depositing a third polysilicon layer on the emitter region, the third polysilicon layer being formed on an area wider than the emitter region; and

forming self-aligned contact holes to form electrodes through the contact holes.

Preferably, the step of etching the silicon substrate is performed using a difference of etching rate between the first patterned insulating layer and the silicon substrate.

In preferred embodiments, the step of injecting the impurity of the second conductivity type is performed using a diffusion difference between the second patterned insulating layer and the silicon substrate.

Preferably, the step of polishing the first polysilicon layer is performed by chemical-mechanical polishing utilizing a polishing speed difference between the first polysilicon layer and the first oxide layer.

According to a still further another aspect of the present invention there is provided a method of fabricating a pillar bipolar transistor, the method comprising the steps of:

etching a silicon substrate of a first conductivity type using a first patterned insulating layer as a mask to form first and second

pillar structures separated by a trench region therein;

injecting an impurity of a second conductivity type using a second patterned insulating layer as a mask to form an emitter region under the first and second pillar structures and in the second pillar structure;

sequentially depositing a first oxide layer and a first polysilicon layer thereon;

polishing the first polysilicon layer using the first oxide layer as a polishing stopper;

removing a portion of the first polysilicon layer and a portion of the first oxide layer to define an extrinsic base region;

etching the oxide layer formed on both sides of the first pillar structure to a predetermined depth to define a connecting portion and forming a buried polysilicon therein to form the connection portion;

sequentially depositing a second oxide layer and a second polysilicon layer thereon;

polishing the second polysilicon layer using the second oxide layer as a polishing stopper;

removing the second oxide layer formed only upward the first pillar structure to expose a surface of the first pillar structure;

injecting an impurity of the first conductivity type in the first pillar structure to form a base region at a centre portion thereof;

injecting an impurity of the second conductivity type to form a collector region at an upper portion of the first pillar structure;

depositing a third polysilicon layer on the collector region, the third polysilicon layer being formed on an area wider than the collector region; and

forming self-aligned contact holes to form electrodes through the contact holes.

In such pillar bipolar transistors, the intrinsic base can be further reduced in size, because an electrical connection portion is provided between the intrinsic base and an extrinsic base.

Also, the active region can be formed in self-alignment, thereby allowing integration thereof to be enhanced. Parasitic junction capacitance between the base and the collector or between the base and the emitter can be reduced by forming the active region in self-alignment.

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1 is a cross-sectional view showing the construction of a bipolar transistor which is fabricated by a previously proposed method;

Figure 2 is a cross-sectional view showing the construction of a pillar bipolar transistor which is fabricated by another previously proposed method;

Figure 3 is a cross-sectional view showing the construction of a pillar bipolar transistor which is fabricated by the method of one embodiment of the present invention; and

Figures 4A through 4K are cross-sectional views used for explaining the steps for fabricating the pillar bipolar transistor of Figure 3.

Figure 3 is a cross-sectional view of a pillar bipolar transistor which is fabricated in accordance with one embodiment of the present invention.

As shown in Figure 3, a semiconductor substrate 21 is provided with a trench region having at least three recess portions, and first and second pillar structures 10, 20 formed between the trench regions. A collector region (or, an emitter region) is formed under the first and second pillar structures 10, 20 and in the second pillar structure 20, and a thin film for a base electrode or an extrinsic region 24 composed of a polysilicon is buried in the trench regions. Between the extrinsic base 24 and the substrate 21, an oxide layer 34 is formed. Also, at the centre portion of the first pillar structure 10, a base region 27 of a first conductivity type is formed. A connection portion 25 is formed at both sides of the first pillar structure 10, and an emitter region 28 (or the collector region) of a second conductivity type is formed at an upper portion of the first pillar structure 10. Each electrode is formed at a portion of each of the extrinsic base region 24, the emitter (or, collector) region 28, and the collector (or, emitter) 23.

In the pillar bipolar transistor as described above, a conductive thin film 26 wider than the emitter may be formed in order that a contact hole is easily provided for interconnection between the emitter (or, collector) 28 and the emitter electrode 29. The conductive thin film 26 is composed of a polysilicon layer containing an impurity of

the second conductivity type.

Hereinafter, the method for fabricating the pillar bipolar transistor of Figure 3 will be described in detail with reference to Figures 4A through 4K. In Figures 4A through 4K, component elements having similar functions to the component elements of the pillar bipolar transistor shown in Figure 3 are indicated by the same reference numerals.

Referring to Figure 4A, on a p-type silicon substrate 21, an oxide layer is formed, and then a patterning of the oxide layer is performed to form a first patterned oxide layer 32 and define a trench region. Next, an anisotropic etching step is performed using the first patterned oxide layer as an etching mask to form first and second pillar structures 10, 20 separated by the trench portion.

In the etching step, the substrate 21 is etched due to a difference between etching rates of the first patterned oxide layer 32 and the substrate 21.

In Figure 4B, after removal of the patterned oxide layer 32 other than the oxide layer formed only on the first pillar structure 10, an oxide layer is formed thereon, and then the oxide layer is patterned to form a second patterned oxide layer 33 and define a subcollector region. Next, using the second patterned oxide layer 33 as a mask, an impurity injection is carried out to form a collector layer 23 (or, emitter) by injected an impurity to a high concentration. In the impurity injection step, the collector layer 23 is formed under the first and second pillar structures 10, 20 and in the second pillar structure 20 due to an impurity diffusion difference between the second patterned oxide layer 33 and the substrate 21.

As shown in Figure 4C, after removal of all the oxide layers 32, 33, an oxide layer 34 is formed thereon. A polysilicon layer 24' thicker than a step between the trench and the pillar structure is deposited thereon. Next, chemical-mechanical polishing is performed to polish the polysilicon layer 24' up to a surface of the oxide layer 34, as shown in Figure 4D. In the polishing for planarization, the oxide layer 34 is used as a polishing stopper.

With reference to Figure 4E, a dry-etching is carried out to remove a portion of the polysilicon layer 24' and a portion of the oxide layer 34. As a result, a thin film for a base electrode or an

extrinsic base 24 is formed in the trench region. Next, only the oxide layer 34 formed on both sides of the first pillar structure 10 is selectively removed to define a connecting region 25'. In the connection region 25', a polysilicon layer is buried to form a connection portion 25 for electrically connecting a base, i.e. an intrinsic base to be formed by a following process, with the extrinsic base 24, as shown in Figure 4F.

Subsequently, after formation of an oxide layer 36 as shown in Figure 4G, a polysilicon layer 35 is deposited thereon, and then a chemical-mechanical polishing is performed using the oxide layer 36 as a polishing stopper to obtain a planarized surface, as shown in Figure 4H.

In Figure 4I, after removal of only the oxide layer 36 formed on top of the first pillar structure 10, an injection of a p-type impurity is performed to form the intrinsic base 27 at a centre portion of the first pillar structure 10. Then, the intrinsic base 27 is electrically connected with the extrinsic base 24'. Also, an n-type impurity is injected to the first pillar structure 10 to form an emitter region 28 (or collector) at an upper portion of the first pillar structure 10.

In addition, after removal of the polysilicon layer 35, a polysilicon layer 26 doped with an n-type impurity is formed on the emitter region (or collector) 28, as shown in Figure 4J. The polysilicon layer 26 is formed over an area wider than the emitter region 28.

Finally, as shown in Figure 4K, a passivation layer 27 is deposited thereon, and then a self-aligned contact hole formation step is performed to form openings on each portion of the extrinsic base 24, the polysilicon layer 26 and the collector (or emitter) 23. Next, a metallization step is performed to form wiring electrodes 29, and therefore the fabrication sequence of the pillar bipolar transistor is completed.

As described above, an intrinsic base of the pillar bipolar transistor fabricated by the method of the present invention can be further reduced in size, because an electrical connection portion is provided between the intrinsic base and an extrinsic base.

In the pillar bipolar transistor, also, an active region thereof can be formed in self-alignment, thereby allowing integration thereof

to be enhanced. Parasitic junction capacitance between the base and the collector or between the base and the emitter can be reduced by forming the active region in self-alignment.

In addition, according to the method of this embodiment of the present invention, a pillar bipolar transistor having good bidirectional operation characteristic can be fabricated.

Furthermore, because of a reduction of the parasitic capacitance and enhancement of the good bidirectional operation characteristic, the pillar bipolar transistor is suited for use in integrated circuits of a low-power consumption.

In the method, it is easier to perform a multi-layer interconnection because of the good planarization of the surfaces. More particularly, an extrinsic base region to be electrically connected with an intrinsic base region in the pillar and a self-aligned contact holes for interconnection of electrode can be easily formed.

It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope of this invention.

CLAIMS

1. A pillar bipolar transistor, comprising:

a semiconductor substrate of a first conductivity type having at least three trench regions, and first and second pillar structures formed between the trench regions;

a collector region formed under the first and second pillar structures and in the second pillar structure, and doped with an impurity of a second conductivity type;

a extrinsic base region buried in the trench regions;

an oxide layer formed between the extrinsic base region and the substrate;

an intrinsic base region of the first conductivity type formed at a centre portion of the first pillar structure;

a connecting portion formed between the extrinsic base region the intrinsic base region to electrically connect the extrinsic base region with the intrinsic base region;

an emitter region of the second conductivity type formed at an upper portion of the first pillar structure; and

electrodes formed through contact holes on the emitter, collector and base region.

2. A pillar bipolar transistor as claimed in claim 1, further comprising a conductive thin film wider than and formed on top of the emitter so as to make formation of a contact hole easier.

3. A pillar bipolar transistor as claimed in claim 2, wherein the conductive thin film is composed of polysilicon containing an impurity of the second conductivity type.

4. A pillar bipolar transistor as claimed in any one of claims 1 and 2, wherein the extrinsic base region is composed of polysilicon.

5. A pillar bipolar transistor, comprising:

a semiconductor substrate of a first conductivity type having at least three trench regions, and first and second pillar structures formed between the trench regions;

an emitter region formed under the first and second pillar structures and in the second pillar structure, and doped with an impurity of a second conductivity type.

an extrinsic base region buried in the trench regions;

an oxide layer formed between the extrinsic base region and the substrate;

an intrinsic base region of the first conductivity type formed at a centre portion of the first pillar structure;

a connection portion formed between the extrinsic base region the intrinsic base region to electrically connect the extrinsic base region with the intrinsic base region;

a collector region of the second conductivity type formed at an upper portion of the first pillar structure; and

electrodes formed through contact holes on the emitter, collector and base region.

6. A method of fabricating a pillar bipolar transistor, the method comprising the steps of:

etching a silicon substrate of a first conductivity type using a first patterned insulating layer as a mask to form first and second pillar structures separated by a trench region therein;

injecting an impurity of a second conductivity type using a second patterned insulating layer as a mask to form a collector region under the first and second pillar structures and in the second pillar structure;

sequentially depositing a first oxide layer and a first polysilicon layer thereon;

polishing the first polysilicon layer using the first oxide layer as a polishing stopper;

removing a portion of the first polysilicon layer and a portion of the first oxide layer to define an extrinsic base region;

etching the oxide layer formed on both sides of the first pillar structure to a predetermined depth to define a connecting portion and forming a buried polysilicon therein to form the connection portion;

sequentially depositing a second oxide layer and a second polysilicon layer thereon;

polishing the second polysilicon layer using the second oxide

layer as a polishing stopper;

removing only the second oxide layer formed on top of the first pillar structure to expose a surface of the first pillar structure;

injecting an impurity of the first conductivity type in the first pillar structure to form a base region at a centre portion thereof;

injecting an impurity of the second conductivity type to form an emitter region at an upper portion of the first pillar structure;

depositing a third polysilicon layer on the emitter region, the third polysilicon layer being formed on an area wider than the emitter region; and

forming self-aligned contact holes to form electrodes through the contact holes.

7. A method as claimed in claim 6, wherein the step of etching the silicon substrate is performed using a difference of etching rate between the first patterned insulating layer and the silicon substrate.

8. A method as claimed in any one of claims 6 and 7, wherein the step of injecting the impurity of the second conductivity type is performed using a diffusion difference between the second patterned insulating layer and the silicon substrate.

9. A method as claimed in any one of claim 6, 7 and 8, wherein the step of polishing the first polysilicon layer is performed by chemical-mechanical polishing utilizing a polishing speed difference between the first polysilicon layer and the first oxide layer.

10. A method of fabricating a pillar bipolar transistor, the method comprising the steps of:

etching a silicon substrate of a first conductivity type using a first patterned insulating layer as a mask to form first and second pillar structures separated by a trench region therein;

injecting an impurity of a second conductivity type using a second patterned insulating layer as a mask to form an emitter region under the first and second pillar structures and in the second pillar structure;

sequentially depositing a first oxide layer and a first

polysilicon layer thereon;

polishing the first polysilicon layer using the first oxide layer as a polishing stopper;

removing a portion of the first polysilicon layer and a portion of the first oxide layer to define an extrinsic base region;

etching the oxide layer formed on both sides of the first pillar structure to a predetermined depth to define a connecting portion and forming a buried polysilicon therein to form the connection portion;

sequentially depositing a second oxide layer and a second polysilicon layer thereon;

polishing the second polysilicon layer using the second oxide layer as a polishing stopper;

removing the second oxide layer formed only upward the first pillar structure to expose a surface of the first pillar structure;

injecting an impurity of the first conductivity type in the first pillar structure to form a base region at a centre portion thereof;

injecting an impurity of the second conductivity type to form a collector region at an upper portion of the first pillar structure;

depositing a third polysilicon layer on the collector region, the third polysilicon layer being formed on an area wider than the collector region; and

forming self-aligned contact holes to form electrodes through the contact holes.

11. A pillar bipolar transistor substantially as hereinbefore described with reference to Figures 3 and 4A to 4K of the accompanying drawings.

12. A method of fabricating a pillar bipolar transistor substantially as hereinbefore described with reference to Figures 3 and 4A to 4K of the accompanying drawings.

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Patents Act 1977 **Examiner's report to the Comptroller under Section 17** **(The Search report)**	Application number GB 9425735.9
Relevant Technical Fields (i) UK Cl (Ed.N) H1K (KAAL, KAAP, KAAX) (ii) Int Cl (Ed.6) H01L	Search Examiner S J MORGAN Date of completion of Search 14 MARCH 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE DATABASE: WPI	Documents considered relevant following a search in respect of Claims :- 1-4, 6-9

Categories of documents

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Y: Document indicating lack of inventive step if combined with one or more other documents of the same category.

A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages	Relevant to claim(s)
X	US 4674173 see whole document	1-4

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